WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first insulation film provided above a semiconductor substrate;

a conductive film selectively provided at least on a bottom of a groove section formed in the first insulation film; and

a wiring layer formed on the conductive film so as to have a space region between the wiring layer and at least one sidewall of the groove section.

2. The semiconductor device according to claim 1, wherein the conductive film is barrier metal and has resistivity that is higher than that of the wiring layer.

3. The semiconductor device according to claim 1, further comprising a second insulation film formed above the space region, the second insulation film being different from the first insulation film.

4. The semiconductor device according to claim 1, further comprising a third insulation film formed on a sidewall of the groove section, the third insulation film being different from the first and second insulation films.

5. A semiconductor device comprising:

a first insulation film provided above a semiconductor substrate;

a wiring layer buried in the first insulation

film;

a conductive film provided at least on a bottom of the wiring layer; and

a fourth insulation film formed on at least one side of the wiring layer, the fourth insulation film being different from the first insulation film.

6. The semiconductor device according to claim 5, wherein the conductive film is barrier metal and has resistivity that is higher than that of the wiring layer.

7. A semiconductor device comprising:

an insulation film provided above a semiconductor substrate;

a wiring layer buried in the insulation film;

a first conductive film provided at least on a bottom of the wiring layer; and

a second conductive film formed on at least one side of the wiring layer.

8. The semiconductor device according to claim 7, wherein the first conductive film is barrier metal and has resistivity that is higher than that of the wiring layer.

9. The semiconductor device according to claim 7, wherein the second conductive film has resistivity that is almost equal to that of the wiring layer.

10. A semiconductor device comprising:

a first insulation film provided above

a semiconductor substrate;

at least two wiring layers buried in the first insulation film;

a first conductive film provided on a bottom of each of the wiring layers;

a fifth insulation film formed on at least one side of each of the wiring layers; and

a contact plug provided between the two wiring layers with the fifth insulation film interposed therebetween.

11. The semiconductor device according to claim 10, wherein the first conductive film is barrier metal and has resistivity that is higher than that of the two wiring layers.

12. The semiconductor device according to claim 10, wherein the two wiring layers are bit lines.

13. The semiconductor device according to claim 10, wherein the contact plug is formed in self-alignment with the fifth insulation film.

14. The semiconductor device according to claim 10, wherein the contact plug includes barrier metal of a third conductive film and a storage node contact of a fourth conductive film.

15. The semiconductor device according to claim 10, wherein a space region is provided between at least one side of each of the two wiring layers and the fifth insulation film.

16. A method of manufacturing a semiconductor device, comprising the steps of:

forming a groove section in a first insulation film provided above a semiconductor substrate;

forming a first conductive film on the first insulation film along the groove section;

forming a buried wiring layer in the groove section with the first conductive film interposed therebetween; and

selectively removing the first conductive film from at least one sidewall portion of the groove section to form a space region between the sidewall portion and one side of the wiring layer.

17. The method according to claim 16, wherein the first conductive film is barrier metal and has resistivity that is higher than that of the wiring layer.

18. The method according to claim 16, further comprising a step of causing the first conductive film of a bottom of the groove section and that of each sidewall of the groove to differ in quality from each other.

19. The method according to claim 16, wherein in the step of forming the wiring layer, the first conductive film and the wiring layer are flattened such that top surfaces of the first conductive film and the wiring layer are almost flush with a top surface of

the first insulation film.

20. The method according to claim 16, further comprising a step of forming a second insulation film on the first insulation film after the step of forming the space region.

21. The method according to claim 20, wherein the second insulation film is poor in being buried in the space region.

22. The method according to claim 16, further comprising a step of forming a third insulation film on a sidewall portion of the groove section after the step of forming the groove section in the first insulation film.

23. The method according to claim 16, further comprising a step of burying a fourth insulation film in the space region.

24. The method according to claim 23, wherein the fourth insulation film is good at being buried in the space region.

25. The method according to claim 16, further comprising a step of burying a second conductive film in the space region.

26. The method according to claim 25, wherein the second conductive film has resistivity that is almost equal to that of the wiring layer.

27. A method of manufacturing a semiconductor device, comprising the steps of:

forming a groove section in a first insulation film provided above a semiconductor substrate;

forming a third insulation film on at least one sidewall portion of the groove section;

forming a first conductive film in the groove section along the third insulation film;

forming a buried wiring layer in the groove section with the first conductive film interposed therebetween; and

selectively removing the third insulation film from at least one sidewall portion of the groove section to form a space region between the sidewall portion and one side of the wiring layer.

28. The method according to claim 27, wherein the first conductive film is barrier metal and has resistivity that is higher than that of the wiring layer.

29. The method according to claim 27, further comprising a step of causing the first conductive film of a bottom of the groove section and that of each sidewall of the groove to differ in quality from each other.

30. The method according to claim 27, wherein in the step of forming the wiring layer, the first conductive film and the wiring layer are flattened such that top surfaces of the first conductive film and the wiring layer are almost flush with a top surface of

the first insulation film.

31. The method according to claim 27, further comprising a step of forming a second insulation film on the first insulation film after the step of forming the space region.

32. The method according to claim 31, wherein the second insulation film is poor in being buried in the space region.

33. A method of manufacturing a semiconductor device, comprising the steps of:

forming at least two groove sections in a first insulation film provided above a semiconductor substrate;

forming a first conductive film on the first insulation film along each of the two groove sections;

forming a buried wiring layer in each of the two groove section with the first conductive film interposed therebetween;

selectively removing the first conductive film from at least one sidewall portion of each of the two groove section; and

forming a contact plug between the two groove sections with a fifth insulation film interposed therebetween.

34. The method according to claim 33, wherein the fifth insulation film is formed on a sidewall portion of each of the two groove sections after the step of

selectively removing the first conductive film.

35. The method according to claim 33, wherein the fifth insulation film is formed on at least one sidewall portion of each of the two groove sections after the step of forming the two groove sections.

36. The method according to claim 35, wherein a space region is provided between the fifth insulation film and the wiring layer.

37. The method according to claim 33, wherein the first conductive film is barrier metal and has resistivity that is higher than that of the wiring layer.

38. The method according to claim 33, wherein the wiring layer is selectively etched such that a level of a top surface of the wiring layer is equal to or lower than that of a top surface of the first insulation film.

39. The method according to claim 38, wherein the wiring layer is a bit line.

40. The method according to claim 33, wherein the contact plug is formed in self-alignment with the fifth insulation film.

41. The method according to claim 33, wherein the contact plug includes barrier metal of a third conductive film and a storage node contact of a fourth conductive film.